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(54) **LOGARITHMIC AMPLIFIER**

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(52) **U.S. Cl.** **327/350; 327/351; 327/352**

(58) **Field of Search** **327/350, 351, 327/352, 358, 359, 361**

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(57) **ABSTRACT**

A parallel-summation logarithmic amplifier is described that uses a novel topology of cascaded and parallel amplifiers to achieve extremely high bandwidth. Included in the topology is a unique delay matching scheme for logarithmic amplifiers that is amenable to fabrication in integrated circuit form. The result is flat group delay over broad frequency ranges and different power levels. The resulting log amplifier is suitable for radar applications and for use in high data rate fiber-optic networks. Also described is a unique design process that yields a set of amplifier gains that closely approximate a logarithm. Also described is the novel idea of using a parallel feedback amplifier (PFA) in piecewise-approximate logarithmic amplifiers. This innovation allows for the design of broadband amplifiers with significantly different gains and similar phase characteristics, which is extremely useful when designing high-frequency logarithmic amplifiers.

32 Claims, 20 Drawing Sheets

